Bibliography

[Bell78] C. G. Bell, A. Kotok, T. N. Hastings, and R. Hill, ‘‘The Evolution of the DECsystem-10,’’ in *Computer Engineering, a DEC View of Hardware Systems Design (Bell, Mudge, and McNamara)*, Digital Press, Bedford, MA (1978).

[Berk91] C. H. v. Berkel, ‘‘Beware the Isochronic Fork,’’ Nat. Lab. Unclassified Report UR 003/91, Philips Research Lab., Eindhoven, The Netherlands (1991).

[Burn87] S. M. Burns and A. J. Martin, ‘‘Syntax-Directed Translation of Concurrent Programs into Self-Timed Circuits,’’ *Advanced Research in VLSI: Proceedings of the Fifth MIT Conference*, Cambridge, MA, pp. 35-50 (March 1987).

[Cade91] Cadence, *Verilog-XL Reference Manual*, Cadence Design Systems, Inc., Lowell, MA (1991).

[Cast82] X. Castillo, S. R. McConnel, and D. P. Siewiorek, ‘‘Derivation and Calibration of a Transient Error Reliability Model,’’ *IEEE Transactions on Computers* **C-31**(7), pp. 658-671 (July 1982).

[Ciac81] M. L. Ciacelli, ‘‘Fault Handling on the IBM 4341 Processor,’’ *11th Fault Tolerant Computing Symposium*, Portland, Maine, pp. 9-12 (June 1981).

[Dall86] W. J. Dally and C. L. Seitz, ‘‘The Torus Routing Chip,’’ *Distributed Computing* **1**(4), pp. 187-196 (October 1986).

[Fran83] E. H. Frank and R. F. Sproull, ‘‘A Self-Timed Static RAM,’’ *Third Caltech Conference on VLSI*, Pasadena, CA, pp. 275-285 (March 1983).

[Henn90] J. L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann, San Mateo, CA (1990).

[Host91] L. B. Hostetler and B. Mirtich, ‘‘DLXsim – A Simulator for DLX,’’ Documentation in the DLX Simulator Software Package (May 1, 1991).

[Jaco90] G. M. Jacobs and R. W. Brodersen, ‘‘A Fully Asynchronous Digital Signal Processor Using Self-Timed Circuits,’’ *IEEE Journal of Solid-*

State Circuits **25**(6), pp. 1526-1537 (December 1990).

[Mart85] A. J. Martin, ‘‘The Design of a Self-Timed Circuit for Distributed Mutual Exclusion,’’ *1985 Chapel Hill Conference on VLSI*, Chapel Hill, NC, pp. 245-260 (March 1985).

[Mart86] A. J. Martin, ‘‘Compiling Communicating Processes into Delay-Insensitive VLSI Circuits,’’ *Distributed Computing* **1**(4), pp. 226-234 (October 1986).

[Mart89] A. J. Martin, S. M. Burns, T. K. Lee, D. Borkovic, and P. J. Hazewindus, ‘‘The First Asynchronous Microprocessor: The Test Results,’’ *Computer Architecture News* **17**(4), pp. 95-110 (June 1989).

[Meng89] T. H.-Y. Meng, R. W. Brodersen, and D. G. Messerschmitt, ‘‘Automatic Synthesis of Asynchronous Circuits from High-Level Specifications,’’ *IEEE Transactions on Computer-Aided Design* **8**(11), pp. 1185-1205 (November 1989).

[Moln85] C. E. Molnar, T.-P. Fang, and F. U. Rosenberger, ‘‘Synthesis of Delay-Insensitive Modules,’’ *1985 Chapel Hill Conference on VLSI*, Chapel Hill, NC, pp. 67-86 (March 1985).

[Patt83] D. A. Patterson, P. Garrison, M. Hill, D. Lioupis, C. Nyberg, T. Sippel, and K. V. Dyke, ‘‘Architecture of a VLSI Instruction Cache For a RISC,’’ *10th Annual Symposium on Computer Architecture*, Stockholm, Sweden, pp. 108-116 (June 1983).

[Seit80] C. L. Seitz, ‘‘System Timing,’’ in *Introduction to VLSI Systems (Mead and Conway)*, Addison-Wesley, Reading, MA (1980).

[Siew92] D. P. Siewiorek, D. Ciplickas, J. Willis, A. Gupta, and J. Quinlan, ‘‘Laboratory Experiences with Verilog Simulation in an Undergraduate Computer Architectdure Course,’’ *Proceedings of the Annual Open Verilog International User Group Meeting*, Santa Clara, CA (March 24-25, 1992).

[Stro85] R. E. Strom and S. Yemini, ‘‘Optimistic Recovery in Distributed Systems,’’ *ACM Transactions on Computer Systems* **3**(3), pp. 204-226 (August 1985).

[Suth89] I. E. Sutherland, ‘‘Micropipelines,’’ *Communications of the ACM* **32**(6), pp. 720-738 (June 1989).

[Tami88] Y. Tamir, M. Tremblay, and D. A. Rennels, ‘‘The Implementation and Application of Micro Rollback in Fault-Tolerant VLSI Systems,’’ *18th Fault-Tolerant Computing Symposium*, Tokyo, Japan, pp. 234-239 (June 1988).

[Tami90a] Y. Tamir and M. Tremblay, ‘‘High-Performance Fault-Tolerant VLSI Systems Using Micro Rollback,’’ *IEEE Transactions on Computers* **C-39**(4), pp. 548-554 (April 1990).

[Tami90b] Y. Tamir, M. Liang, T. Lai, and M. Tremblay, ‘‘The UCLA Mirror Processor: A Building Block for Self-Checking Self-Repairing Computing Nodes,’’ CS Department Technical Report #CSD-900040, University of California, Los Angeles, CA (November 1990).

[Trem89] M. Tremblay and Y. Tamir, ‘‘Support for Fault Tolerance in VLSI Processors,’’ *International Symposium on Circuits and Systems*, Portland, OR, pp. 388-393 (May 1989).

[TRW92] TRW, ‘‘RH32 Spaceborne Data Processor,’’ Preliminary Product Announcement, TRW Space Communications Division, Redondo Beach, CA (March 1992).

[Wils92] R. Wilson, ‘‘VLSI Meet Sees CPUs Speed Up,’’ *Electronic Engineering Times*, p. 1 (June 8, 1992).

[Wint92] K. D. Winters, ‘‘ASIC Design Experience in Undergraduate Logic Design and Computer Architecture Courses,’’ Engineering Research Laboratory Report #92005, Montana State University, Bozeman, MT (April 10, 1992).